REMARKS

Claims 1-17 are in the application. Claims 18-20 were canceled without prejudice in response to a requirement for restriction.

DRAWINGS

The drawings were objected to because FIG. 1 was not designated by a legend such as "Prior Art." The examiner's permission is requested to amend the drawings to include a legend designating FIG. 1 as "Prior Art." In addition, applicants request the examiner's permission to amend FIG. 3 by deleting reference character 122 because it does not appear in the Detailed Description. A red-lined set of drawings having the requested changes is included herewith for the examiner's approval.

REJECTION OF CLAIMS 1-17 UNDER 35 U.S.C. § 103(a)

Claims 1-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Background of the Invention in view of U.S. Patent No. 6,780,741 to Chen et al. This rejection is respectfully traversed.

Applicants teach on page 1, line 22, and continuing to page 2, line 6, that a layer of dielectric material 18 is formed on major surface 14. Floating gates 20 and 22 are disposed on portions of dielectric layer 18 and are spaced apart from each other by a gap. The initial width of the gap is indicated by arrows 24. An Oxide-Nitride-Oxide ("ONO") dielectric structure 19 is formed on floating gates 20 and 22. A layer of polysilicon 28 having a surface 30 is disposed on dielectric structure 19. Because floating gates 20 and 22 create a surface topography over surface 14, a void 32 forms in the portion of polysilicon layer 28 between floating gates 20 and 22, i.e., in the region of the gap. Void 32 degrades the performance of the devices comprising EEPROM 10 and, therefore, it degrades the performance of EEPROM 10. In addition, when layers such as polysilicon layer 28 are formed, their surfaces are not smooth but have a surface roughness associated with them. Typically, this surface roughness has a Root Mean Square (RMS) surface roughness of greater than 75 Angstroms (Å). As the transistors are made smaller,

this surface roughness adversely affects subsequent photolithographic steps. For example, a photoresist layer 34 deposited on polysilicon layer 28 having a rough surface 30, will have a "wavy," i.e., non-planar surface. When photoresist layer 34 is exposed to light, the waviness increases the reflection of light within photoresist layer 34, which degrades the quality of the pattern formed in the photoresist layer. For small geometry devices, this degradation may lower the performance of the transistors or decrease their yield.

Chen et al. teach in column 3, lines 19-35, a process to alter the grain structure of polysilicon seed layer 3a, from a columnar grain layer to a random grain layer, comprised of small random polysilicon grains, is next addressed. An in situ anneal procedure is performed in the same furnace used for deposition of polysilicon seed layer 3a, at a temperature between about 600 to 660° C., in a hydrogen ambient, for a time between about 1 to 3 min. The anneal procedure converts large columnar grains 20, in polysilicon seed layer 3a, to small, random grains 30. Polysilicon seed layer 3b, shown schematically in FIG. 2A, now features smoother surfaces when compared to the rougher surfaces of pre-annealed, polysilicon seed layer 3a, thus decreasing vertical electric scattering, improving carrier mobility, as well as providing an easier layer to experience subsequent definition procedures. FIG. 2B, schematically illustrates polysilicon seed layer 3b, now comprised with small, random grains 30.

Chen et al. further teach in column 4, lines 13-34, that the presence of columnar grains 40, in polysilicon cap layer 5a, results in a rough top surface topography which reduces the ability to define narrow width gate structures in polysilicon cap layer 5a, via photolithographic and dry etching procedures. Therefore another low temperature anneal procedure, again performed in situ, in the same furnace used for deposition of polysilicon cap layer 5a, is performed to alter the columnar grain structure in polysilicon cap layer 5a, to a polysilicon layer comprised with smaller, random grains. The in situ anneal procedure is performed at a temperature between about 600 to 660° C., for a time between about 1 to 3 min, in a hydrogen ambient. The result of this procedure is the evolution of polysilicon cap layer 5b, schematically shown in FIG. 5A, now comprised with small, random grains 50, schematically shown in FIG. 5B. The in situ anneal procedure in addition to altering the grain structure of the polysilicon layer and providing a smooth surface for subsequent definition procedures, also allows activation of dopants in polysilicon$_{(1-x)}G_x$ layer 4 to occur. Without the presence of germanium in

polysilicon$_{(1-x)}$Ge$_x$ layer 4, the activation of dopants would have had to be accomplished at a higher temperature then the in situ anneal temperature.

Chen et al. teach in column 4, lines 35-40, that if desired the in situ anneal procedure applied after deposition of polysilicon seed layer 3a, can be omitted, with the in situ anneal procedure performed after deposition of polysilicon cap layer 5a, used to alter the columnar grain structure of polysilcon layer 3a, to the random grains structure of polysilicon seed layer 3b.

Thus, Chen et al. teach altering the grain structure of polysilicon by converting polysilicon having a columnar grain structure into polysilicon having a grain structure that is random.

Applicants, on the other hand, teach on page 5, lines 13-19, that referring to FIG. 5, that semiconductor component 100 is annealed in a hydrogen (H_2) ambient to redistribute or reposition the silicon atoms of polysilicon layer 132 and form a void-free polysilicon layer 138 having a smoothed surface 140 and a thickness of less than about 300 Å. Redistribution of the silicon atoms fills void 136 and any other void that may have formed in polysilicon layer 132 and smoothes surface 134 such that it has an RMS surface roughness that is preferably less than about 50 Å and even more preferably less than about 20 Å.

Applicants further teach on page 6, lines 1-5, that with reference to FIG. 6, layer of polysilicon 142 is annealed in a hydrogen ambient to redistribute or reposition the silicon atoms of polysilicon layer 142, thereby forming an annealed polysilicon layer 146 having a smoothed surface 148 and a thickness ranging from about 1,000 Å to about 1,500 Å. Accordingly, applicants' claim 1 calls for, among other things, forming a first polysilicon layer over the first and second surface features and redistributing the first polysilicon layer in at least the region between the first and second surface features. Applicants' claim 9 calls for, among other things, forming a first layer of polysilicon over the first and second conductors and repositioning atoms of the first layer of polysilicon. At least these features of applicants' claims 1 and 9 are not taught or suggested in the relied on references, either alone or in combination. Accordingly, the relied on references taken together or alone are deficient in making obvious applicants' claims 1 and 9.

Claims 2-8 depend either directly or indirectly from claim 1 and are believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 1. Claim 4 further sets out heating the first polysilicon layer to a temperature ranging

between approximately 750 degrees Celsius and approximately 1,100 degrees Celsius. Claim 8 further sets out annealing the second polysilicon layer in a hydrogen ambient and by heating the second polysilicon layer to a temperature of at least 750 degrees Celsius. At least these limitations of applicants' claims 4 and 8 are not taught or suggested by the relied on references, either alone or in combination, further precluding obviousness of applicants' claims 4 and 8.

Claims 10-17 depend either directly or indirectly from claim 9 and are believed allowable over the relied on references, either alone or in combination, for at least the same reasons as claim 11. Claim 13 further sets out that repositioning atoms of the first layer of polysilicon comprises heating the first layer of polysilicon to a temperature of at least 750 degrees Celsius. At least this limitation of applicants' claim 13 is not taught or suggested by the relied on references, either alone or in combination, further precluding obviousness of applicants' claim 13.

As stated hereinbefore, Chen et al. teach annealing at a temperature between about 600 to 660° C. Applicants' claims 4, 8, and 13 call for annealing at a temperature of at least 750 degrees Celsius. It was stated in the Office action that it would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the first polysilicon layer that includes heating the first polysilicon layer to a temperature ranging between approximately 750 degrees Celsius and approximately 1,100 degrees Celsius because it was held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum working ranges involve only routine skill in the art. However, it is respectfully submitted that for Chen et al. to anneal at a higher temperature would have destroyed the function of their invention. More particularly, Chen et al. teach in column 4, lines 27-35, that the in situ anneal procedure in addition to altering the grain structure of the polysilicon layer and providing a smooth surface for subsequent definition procedures, also allows activation of dopants in polysilicon$_{(1-x)}$G$_x$ layer 4 to occur. Without the presence of germanium in polysilicon$_{(1-x)}$Ge$_x$ layer 4, the activation of dopants would have had to be accomplished at a higher temperature then the in situ anneal temperature. Thus, Chen et al. could not achieve the objective of an in situ anneal had they used a higher temperature. It is respectfully submitted that modifying a prior art reference to support an obviousness rejection is impermissible when that modification would destroy the function of the prior art reference. Accordingly, modifying applicants' Background of the Invention in view

Chen et al. to arrive at the limitations of applicants' claims 4, 8, and 13 lacks the supposition of obviousness as set forth under 35 U.S.C. § 103.

Because Chen et al. teach the use of germanium to accomplish an in situ anneal, which is carried out at temperatures ranging from 600° C to 660° C, it is believed that Chen et al. teach away from applicants' temperature limitations of claims 4, 8, and 13. It is respectfully submitted that a prior art reference that teaches away from a claim limitation cannot support an obviousness rejection, further precluding obviousness of claims 4, 8, and 13.

CONCLUSION

No new matter is introduced by the amendments herein. Based on the foregoing, applicants believe that all claims under consideration are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,

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